CLAIMS

Please amend the claims as follows:

1.-16. (canceled)

17. (currently amended) A ~~The~~ processor ~~of Claim 3~~, comprising:

a plurality of registers;

instruction processing circuitry that fetches an instruction sequence for execution, said instruction sequence including a load instruction and a preceding instruction that precedes said load instruction in program order, wherein said instruction processing circuitry ~~and~~, after fetching said instruction sequence for execution and prior to dispatching said load instruction for execution and responsive to detecting said load instruction within said fetched instruction sequence, translates said load instruction into separately executable prefetch and register operations; and

execution circuitry that performs at least said prefetch operation out-of-order with respect to said preceding instruction to prefetch data and subsequently separately executes said register operation to place said data into a register among said plurality of registers specified by said load instruction, wherein said execution circuitry performs said prefetch operation by calculating a speculative target memory address utilizing contents of at least one register without regard for whether said contents will be modified between calculation of said speculative target memory address and performing said register operation, and by thereafter initiating a fetch of said data from a memory location associated within said speculative target memory address.

18. (currently amended) A ~~The~~ method ~~of Claim 10~~, said method comprising:

fetching an instruction sequence for execution, said instruction sequence including a load instruction and a preceding instruction that precedes said load instruction in program order;

in response to fetching said instruction sequence for execution and prior to execution of said load instruction, instruction processing circuitry detecting said load instruction within said

fetched instruction sequence and translating said load instruction into separately executable prefetch and register operations;

performing at least said prefetch operation out-of-order with respect to said preceding instruction to prefetch data, wherein performing said prefetch operation comprises:

calculating a speculative target memory address utilizing contents of at least one register without regard for whether said contents will be modified between calculation of said speculative target memory address and performing said register operation; and

thereafter initiating a fetch of said data from a memory location associated within said speculative target memory address; and

thereafter, separately executing said register operation to place said data into a register among said plurality of registers specified by said load instruction.